

WHAT IS CLAIMED

1. A method of selectively coupling digital communication packets, that are presented to virtual circuit input ports of a packet switch, through said switch to virtual circuit output ports thereof, said  
5 method comprising the steps of:

(a) providing a packet analysis mechanism, which is operative to analyze contents of a packet presented to said packet switch and to controllably route said respective packet to a selected virtual circuit output  
10 port of said packet switch, said packet analysis mechanism being configured as a virtual function packet flow control mechanism which is operative to execute a prescribed data flow path routine that calls successive virtual functions, which nominally encounter no  
15 conditional branching or function replacement; and

(b) presenting a packet coupled to a virtual circuit input port to said packet analysis mechanism and thereby causing said packet to be routed to a virtual circuit output port of said packet switch.

2. The method according to claim 1, wherein step (a) comprises storing said packet analysis mechanism in an instruction cache of a communication control processor of a frame engine for said packet switch.

3. the method according to claim 2, wherein step  
(a) further includes storing in memory exclusive of said  
instruction cache an auxiliary processing routine that is  
configured to handle exceptions to the nominal data flow  
5 path of said packet analysis mechanism.

4. A packet switch control mechanism for  
controlling the selective coupling of digital  
communication packets presented to virtual circuit input  
ports of a packet switch to virtual circuit output ports  
5 thereof comprising:

a packet routing control processor for said packet  
switch, including an instruction cache; and

a packet analysis mechanism, stored in said  
instruction cache and being operative to analyze contents  
10 of a packet presented to said packet switch and to  
controllably route said respective packet to a selected  
virtual circuit output port of said packet switch, said  
packet analysis mechanism being configured as a virtual  
function packet flow control mechanism which is operative  
15 to execute a prescribed data flow path routine that calls  
successive virtual functions, which nominally encounter  
no conditional branching or function replacement.

5. The packet switch control mechanism according to claim 4, further including memory exclusive of said instruction cache for storing an auxiliary processing routine that is configured to handle exceptions to the nominal data flow path of said packet analysis mechanism.

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